REMARKS/ARGUMENTS

Favorable consideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1-20 are presently pending in this application, Claims 1-17 having been amended and Claims 18-20 having been added by the present amendment.

In the outstanding Office Action, Claims 1-17 were rejected under 35 U.S.C. §102(b) as being anticipated by Azuma et al. (U.S. Publication 2004/0108862).

Claims 1-17 have been amended to clarify the subject matter recited therein, and Claims 18-20 have been newly added herein. It is believed that these amendments and additions in the claims find clear support in the specification, claims and drawings as originally filed and that no new matter is added thereby. If, however, the Examiner disagrees, the Examiner is invited to telephone the undersigned who will be happy to work in a joint effort to derive mutually satisfactory claim language.

Before addressing the outstanding art rejections, a brief summary of Claims 1 and 6 as currently amended is believed to be helpful. Claim 1 is directed to a multilayer printed wiring board and includes a core substrate, a first conductor layer having conductor circuits formed on the core substrate, an interlayer insulating layer formed over the first conductor layer and the core substrate, a second conductor layer having conductor circuits formed on the interlayer insulating layer, and a via hole structure electrically connecting one of the conductor circuits of the first conductor layer and one of the conductor circuits of the second conductor layer. The first conductor layer on the core substrate has a thickness which is larger than a thickness of the second conductor layer on the interlayer insulating layer. Claim 6 is directed to a multilayer printed wiring board and includes a core substrate comprising a multilayer core substrate comprising not less than three layers including one or more inner conductor layers having conductor circuits, a conductor layer having conductor circuits

formed over the core substrate, an interlayer insulating layer formed over the conductor layer and the core substrate, and a through hole structure formed through the interlayer insulating layer and electrically connecting one of the conductor circuits of the inner conductor layer and one of the conductor circuits of the conductor layer formed over the core substrate. The inner conductor layer of the core substrate and the conductor layer over the core substrate include a power supply layer or an earth.

The outstanding Office Action asserts that Claims 1-17 are anticipated by Azuma et al. Nevertheless, Azuma et al. teaches neither "a first conductor layer …; a second conductor layer …, wherein said first conductor layer on said core substrate has a thickness which is larger than a thickness of said second conductor layer on said interlayer insulating layer" as recited in amended Claim 1, nor "a core substrate comprising a multilayer core substrate comprising not less than three layers including at least one inner conductor layer having a plurality of conductor circuits …, wherein the at least one inner conductor layer of said core substrate … include[s] a power supply layer or an earth" as recited in Claim 6. On the other hand, Azuma et al. shows a multilayer printed wiring board 170 having a waste substrate portion 71B and a product portion 71A, and according to Figure 23A of Azuma et al., the product portion 71A is simply constructed of interlayer insulating layers 70A, 70B and grounding lines 75 formed between the interlayer insulating layers 70A, 70B. Therefore, the structures recited in Claims 1 and 6 are clearly distinguishable from Azuma et al., and thus the first and second conductor layers as recited in Claim 1 and the core substrate as recited in Claim 6 are not anticipated by or rendered obvious over Azuma et al.

Likewise, Claim 18 recites "a multilayered structure formed on said core substrate and including a first conductor layer having a plurality of conductor circuits formed on said core substrate, at least one interlayer insulating layer formed over said first conductor layer, and a second conductor layer having a plurality of conductor circuits formed on said at least

one interlayer insulating layer, wherein said first conductor layer on said core substrate has a thickness which is larger than a thickness of said second conductor layer on said at least one interlayer insulating layer" and is believed to include subject matter substantially similar to what is recited in Claim 1 to the extent discussed above. Thus, Claim 18 is also distinguishable from Azuma et al.

For the foregoing reasons, Claims 1, 6 and 18 are believed to be allowable. Furthermore, since Claims 2-5, 7-17, 19 and 20 depend directly or indirectly from one of Claims 1, 6 and 18, substantially the same arguments set forth above also apply to these dependent claims. Hence, Claims 2-5, 7-17, 19 and 20 are believed to be allowable as well.

In view of the amendments and discussions presented above, Applicants respectfully submit that the present application is in condition for allowance, and an early action favorable to that effect is earnestly solicited.

Respectfully submitted,

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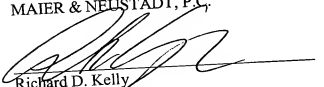

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